

# Agilent 3 – 32 Gb/s programmable stressed BERT solution

Fast, compact, and affordable BER and JTOL testing

Testing InfiniBand EDR communications links requires equipment capable of 25 Gb/s and accurate characterization to strict tolerances. Only a few solutions for BER and JTOL testing at this rate are available today. Until now, those few have been extremely expensive. This often results in multiple designers needing to share the one serial BERT in the lab, delaying their characterization and development schedule.

Agilent Technologies' N4960A serial BERT 32 Gb/s is an affordable alternative for users working at data rates up to 32 Gb/s. The solution is compact, allowing it to be easily transported throughout the lab. But with its low price, a fraction of competing stressed BERTs, you can afford to put one on each bench.

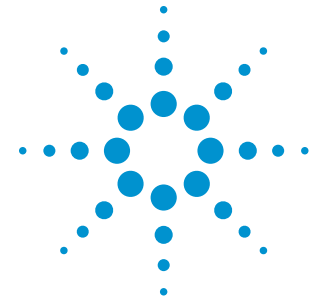
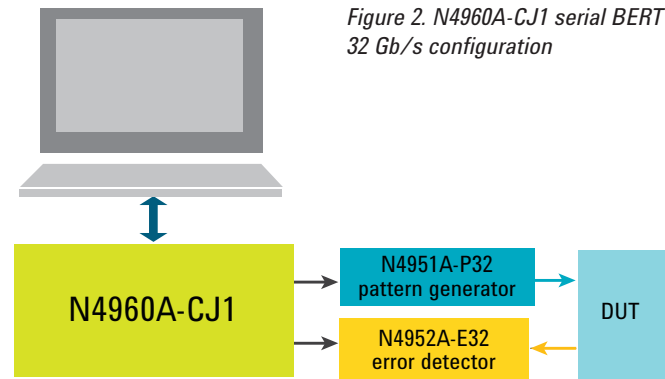


Figure 1. For InfiniBand EDR including TOSA, ROSA, and transceiver testing



## Components – InfiniBand EDR

Product number	Description
N4960A-CJ1 (SSB32J)	Serial BERT 32 and 17 Gb/s
For special applications the system components are available individually	
N4960A-CJ1 (SSB16000J)	Serial BERT controller with jitter injection
N4951A-P32 (PG32)	32 Gb/s pattern generator remote head
N4952A-E32 (ED32)	32 Gb/s error detector remote head



# Quick Fact Sheet

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### Compact architecture

The N4960A-CJ0/N4960A-CJ1 serial BERT controller (SSB16000/SSB16000J) is a platform that forms the basis of the stressed serial BERT. Based on our high performance N4972A clock synthesizer 16 GHz (SCS16000), the N4960A-CJ0/N4960A-CJ1 serial BERT controller (SSB16000/SSB16000J) adds the precision timing and control required for the remote pattern generator and error detector heads.

The concept of remote heads, first introduced by Agilent Technologies with the N4965A multi-channel BERT 12.5 Gb/s (PCB12500), puts the pattern generation and error detection near the device under test, eliminating long cables which degrade the signal. This is especially important at higher data rates.



Figure 3. N4960A serial BERT 32 Gb/s

### Jitter tolerance measurements

The optional JTOL measurement package of the N4980A multi-instrument BERT software (Signal Integrity Studio) performs jitter tolerance compliance and characterization. Setup is quick and easy using the jitter tolerance setup panel that includes an intuitive “point and click” template editor.



Figure 5. Jitter tolerance setup panel

For more information on Agilent amplifiers, please visit [www.agilent.com/find/N4960A](http://www.agilent.com/find/N4960A)

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### Choose the complement of stress sources you need

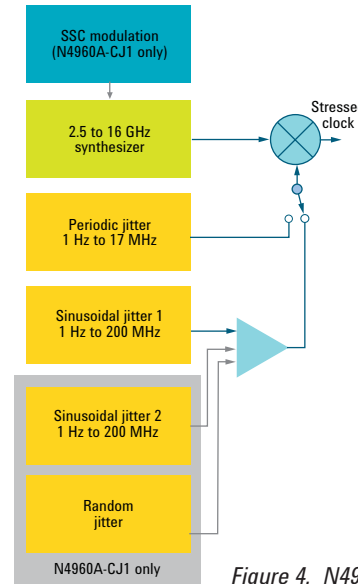


Figure 4. N4960A-CJ1 block diagram

The N4960A series is offered in two models. The base model, N4960A-CJ0 (SSB16000), is ideal for many optical serial data applications, providing a single tone of sinusoidal jitter. Settable over a wide range of frequencies and modulation depth, it facilitates jitter tolerance testing and general receiver characterization.

For applications which require a more complex “stress recipe,” the N4960A-CJ1 (SSB16000J) model includes two independent sources of sinusoidal along with broadband true random jitter sources. The multiple stress generators allow you to build a low level base floor that is a mixture of random and possibly sinusoidal jitter. In addition, all three clock outputs can be modulated with spread spectrum, with a deviation settable up to 1.0 % of the clock frequency (10,000 ppm).

### Programmable patterns

All of the standard patterns used for InfiniBand EDR are built in. For special pattern requirements, programmable patterns up to 8 Mb in length can be easily created with powerful editing tools in the N4980A multi-instrument BERT software (Signal Integrity Studio) and uploaded into the N4960A-CJ0 / N4960A-CJ1 serial BERT controller (SSB16000/SSB16000J).



Figure 6. Programmable patterns window